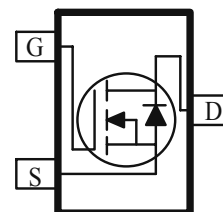
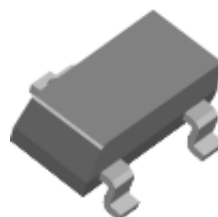


N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are DC-DC converters, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT-23 Surface Mount Package Saves Board Space

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.070 @ $V_{GS} = 4.5V$	2.2
	0.080 @ $V_{GS} = 2.5V$	2.0
	0.120 @ $V_{GS} = 1.8V$	1.8



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	2.2	A
	$T_A = 70^\circ C$		1.8	
Pulsed Drain Current ^b		I_{DM}	8	
Continuous Source Current (Diode Conduction) ^a		I_S	0.6	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	1.25	W
	$T_A = 70^\circ C$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{THJA}	100	$^\circ C/W$
	Steady-State		166	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

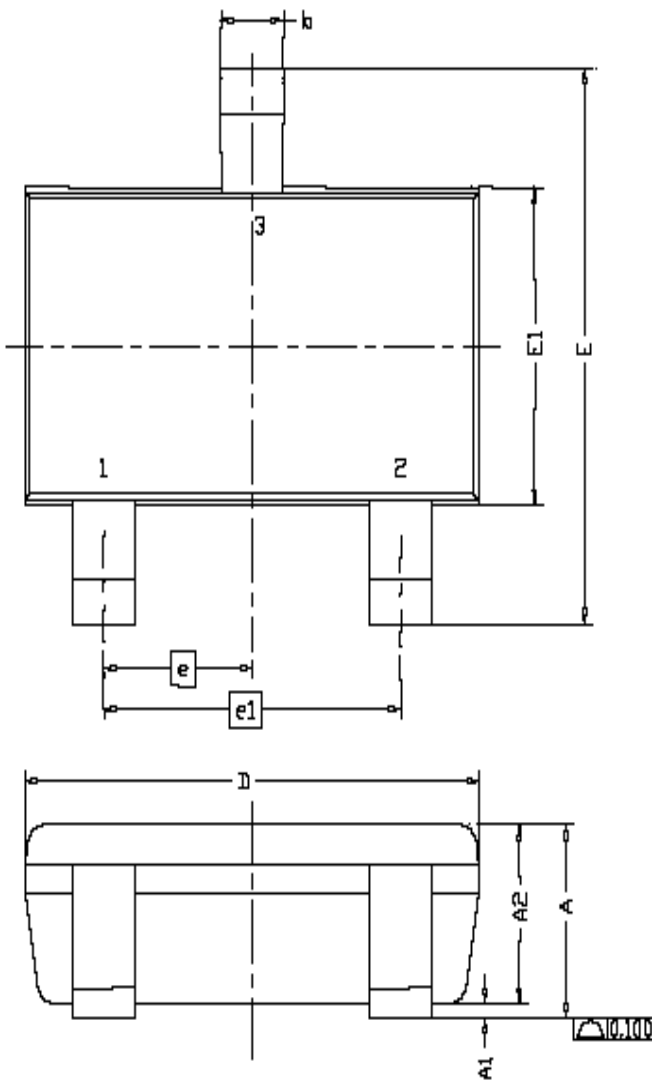
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.70			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 12 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			0.1	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			1	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	5			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 2.2 \text{ A}$			70	m Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 2.0 \text{ A}$			80	
		$V_{GS} = 1.8 \text{ V}, I_D = 1.8 \text{ A}$			120	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 5 \text{ V}, I_D = 2.0 \text{ A}$		11		S
Diode Forward Voltage	V_{SD}	$I_S = 0.6 \text{ A}, V_{GS} = 0 \text{ V}$		0.60		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 2.0 \text{ A}$		4.5		nC
Gate-Source Charge	Q_{gs}			0.89		
Gate-Drain Charge	Q_{gd}			0.95		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, I_D = 1.0 \text{ A}, R_G = 6 \Omega,$ $V_{GS} = 4.5 \text{ V}$		6		ns
Rise Time	t_r			6.5		
Turn-Off Delay Time	$t_{d(off)}$			14		
Fall-Time	t_f			2		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ_1	7°NOM		

